

Patent

NASA Case No.: NPO-20773-CU

IN THE CLAIMS

Please insert the following claims in place of the currently pending claims:

1. (Currently Amended) A method of designing ~~evolving an electronic~~ circuit from plural candidate circuits, comprising:

assigning each one of a plurality of configurable circuit models of different levels of model resolutions to different individual ones of at least a subset of said plural candidate circuits;

producing plural ~~a simulation models~~ for each one of at least said subset of said candidate circuits by configuring each a configurable model ~~assigned to the one candidate circuit~~ in accordance with the one candidate circuit, whereby to produce a plurality of simulation models corresponding to ~~at least said subset of said candidate circuits whose resolutions are distributed among said~~ different levels of model resolutions;

obtaining from each simulation model a fitness function of the corresponding candidate circuit;

ranking said candidate circuits in accordance with said fitness functions;

changing assignments of candidate circuits among said configurable circuit models; and

repeating the steps of producing, obtaining and ranking, whereby to perform them in successive iterations.

2. (Original) The method of Claim 1 wherein said ranking step is followed by a step of eliminating candidate circuits corresponding to inferior ranking.

3. (Original) The method of Claim 2 wherein said ranking step is followed by a step of adding another of said candidate circuits to said subset of candidate circuits.

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4. (Original) The method of Claim 1 wherein the step of assigning is carried out by randomly assigning ones of said plural configurable models to ones of said plural candidate circuits.

5. (Original) The method of Claim 1 wherein the step of assigning is carried out so that each candidate circuit of said subset of candidate circuits is assigned to each of said configurable models of different resolution levels within a finite number of said iterations.

6. (Original) The method of Claim 1 wherein said ranking step includes comparing fitness functions of a candidate circuit obtained during respective ones of said iterations from models of different resolutions.

7. (Original) The method of Claim 6 wherein said ranking step includes retaining a candidate circuit whose fitness functions obtained with models of different resolution levels are superior.

8. (Original) A method of designing evolving an electronic circuit from plural candidate circuits, comprising:

assigning every one of a plurality of configurable circuit models of different levels of model resolutions to each one of at least a subset of said plural candidate circuits;

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producing plural simulation models for each one of at least said subset of said candidate circuits by configuring each configurable model in accordance with the one candidate circuit, whereby to produce a plurality of simulation models for each candidate circuit;

obtaining from the plurality of simulation models of each candidate circuit a plurality fitness functions of the corresponding candidate circuit, and combining said plurality of fitness functions into a single fitness function of the one candidate circuit;

ranking said candidate circuits in accordance with their fitness functions.

9. (Original) The method of Claim 8 wherein said plural configurable models constitute three models corresponding to three different levels of resolution.

10. (Original) The method of Claim 8 wherein said plural configurable models constitute two models corresponding to two different levels of resolution.

11. (Original) The method of Claim 8 wherein said ranking step is followed by a step of eliminating candidate circuits corresponding to inferior ranking.

12. (Original) The method of Claim 11 wherein said ranking step is followed by a step of adding another of said candidate circuits to said subset of candidate circuits.

13. (Original) The method of Claim 8 wherein the step of combining said fitness functions comprises forming an average of said fitness functions.

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14. (Original) The method of Claim 13 wherein said average is a weighted average.
15. (Currently Amended) A method of designing evolving an elecontroic circuit comprising modeling plural candidate circuits at ~~with a heterogeneous mix of models of~~ different levels of resolution over a plurality of iterations.
16. (Currently Amended) The method of Claim 15 wherein each candidate circuit is modeled a plurality of times using models corresponding to all levels of resolution, and wherein fitness functions obtained from said models for each candidate circuit are combined in evaluating the candidate circuit.
17. (Currently Amended) The method of Claim 15 wherein a candidate circuit is modeled at ~~with a single resolution model~~ during a single iteration, different candidates being assigned to models of different resolution levels during a various iterations.
18. (Previously Presented) The method of Claim 17 wherein each candidate circuit is ~~been~~ modeled at all levels of resolution within a finite number of said iterations.
19. (Original) The method of Claim 17 wherein not all candidate circuits are assigned to a different resolution level model at each iteration.
- 20-27. (Canceled)